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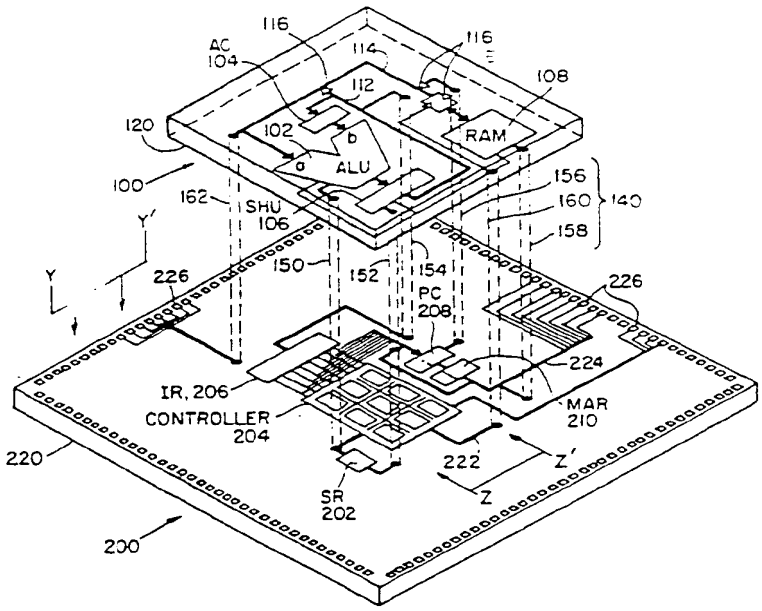


(57) Abstract

A multi-layered structure is fabricated in which a microprocessor is configured in different layers and interconnected vertically through insulating layers which separate each circuit layer of the structure. Each circuit layer can be fabricated in a separate wafer or thin film material and then transferred onto the layered structure and interconnected.

Three-Dimensional Processor Using Transferred Thin Film Circuits

Background of the Invention

Typically, processors are constructed from a variety of very large scale integrated circuit (VLSI) chips used as building blocks in an architecture which can be divided into two components; an instruction processor that supervises the order and decoding of instructions to be executed, and a data processor which performs the operations called for by the instructions on the data. These components are often two different chips mounted on a circuit board, or can be fabricated on a single chip in two dimensional geometry. The instruction processor normally includes a program memory which contains instructions. Each instruction includes a plurality of bits to control the elements within the data processor. In addition, the controller is used to issue addresses that are applied to the program memory to access the instruction sequence to be executed. It is desirable to execute these instructions as fast as possible, preferably in one clock cycle or less. However, due to the geometry of laying out the microprocessor using existing methods, the difficulties in increasing speed also increase the cost and complexity of manufacturing.

Data processors have been categorized as either an 8, 16 or 32-bit device. They are capable of performing arithmetic or logic operations on 8, 16, or 32 bits, respectively. Some processors have limited ability to perform operations on a full-sized word. For example, a 16-bit data processor may be able to perform operations on the least-significant byte (8 bits) of a full-sized 16-bit word. In one such approach, a 16-bit processor is formed from a parallel combination of four-bit

Summary of the Invention

The present invention relates to the structure and fabrication of very large scale integrated circuits, and in particular, to vertically stacked and interconnected circuit elements for data processing, control systems, and programmable computing. A preferred embodiment involves a microprocessor divided into functional blocks, for instance, an Arithmetic Logic Unit (ALU), a controller, memory elements etc., which are fabricated in the same or separate semiconductor wafers and then stacked. Typically, the functional blocks communicate with one another using address, data and control busses. These busses consist of a number of metal wires that are normally routed along the surface of a silicon chip. Typically, the metal wires run in areas of the chip between the functional blocks and take up a considerable amount of real estate, perhaps as much as half that available. In the present invention the functional blocks of the circuit are divided into two or more sections with one section of the circuit on a bulk chip and the remaining blocks on an overlying thin film with components electrically connected through an intervening insulating layer.

Both bulk and thin film semiconductor layers can be incorporated into preferred embodiments of the invention. Circuits can be formed in bulk silicon, silicon-on-insulator (SOI) structures, or in III-V materials such as gallium arsenide, or in composite structures including bulk Si, SOI, and/or thin film GaAs. The various layers of the device can be stacked using an insulating layer that bonds the layers together and conductive interconnects or vertical busses extending through the insulating layer which preferably comprises a polymeric material such as an adhesive. Thermal and electrical shielding can be employed between

deposition is used to connect the lower and upper functional blocks.

Some of the advantages of this three dimensional approach include higher speed and packing density. The speed increases result from at least two areas; the first is the reduction in the length of the busses. On chip circuit speed is limited to some extent by the length of the wires carrying signals around the chip. All wires on the chip have associated capacitances and inductances. Typical treatment of wire lead delays follows from simple transmission line analysis. The longer the leads, the longer the associated delays. In the proposed approach, shorter busses will result in smaller delays and higher speed circuit performance.

The second source of speed improvement is obtained from the SOI itself. The circuit is divided into two halves or into three or more layers in other embodiments. In one embodiment, the first half is a bulk circuit. However, this silicon circuitry can be entirely replaced on SOI.

Improvement in operating speed for SOI circuitry originates from three areas. Perhaps the largest speed enhancement results from the fact the circuit is isolated from the bulk silicon wafer by a thick oxide layer. This reduces individual device capacitance as well as the capacitance associated with the metal and substrate. A second reduction in capacitance is achieved due to a reduction in the exposed source and drain areas common in CMOS circuit components. This is a result of the fact that in SOI, the source/drain implantations are terminated by the oxide layer. This eliminates a large portion of the capacitance associated with the source/drain to well junctions. The final increase in speed has been reported using thin film SOI devices. These are fabricated in silicon layers having

Having completed and tested each of the circuit layers which make up the complete microprocessor, the SOI circuit is transferred to the bulk wafer. A key aspect of the transfer process is that the two or more circuit layers must be aligned to one another. A second aspect of this task is that once combined the circuit halves are integrated. This is performed by etching via holes down to the appropriate interconnection pads, depositing aluminum and patterning the aluminum to create interconnection between the circuits and any routing that may be required.

In embodiments employing more than two layers, interconnections can be performed after transfer of each successive layer or after two or more layers. Such connections can be optical or electrical, and can run externally or through the bonding layers connecting each layer. Connections can also be made between circuit elements on the same layer or different layers using a circuit routing layer. The circuit routing layer can also have circuitry thereon or can be made of an electrical or thermal insulating material such as ceramic or silicon carbide. The circuit routing layer has metalization lines or busses formed on one or both sides. In non-active regions the circuit routing layer can be patterned on one or both sides with a metal that can be connected to ground for further insulation between layers.

A double transfer process can also be used in which a thin film has circuits fabricated followed by transfer onto a second disposable or reusable substrate, back processing of the circuit layer as needed and then transfer onto the stacked structure and interconnecting metalization. Tiling of transferred thin film circuits on each layer of the device can also be employed. These transfer and tiling methods can be used to incorporate

shielding using a grounded metal run patterned over an insulating layer.

FIG. 5B is a cross-sectional view of multi-layer shielding using a metal run patterned on a separate shielding layer.

FIG. 6 is an exploded view of two film layers, each with a multitude of individual dies, being layered together using the single transfer process.

FIG. 7 is a progressional view of layers of film being aligned and epoxied together using the double transfer process, followed by the singulation of an individual multi-layered microprocessor.

FIG. 8 is a perspective view of a completed multi-layer microprocessor, with components which produce the most heat fabricated around the outer perimeter of the first layer.

FIG. 9A is an exploded perspective view demonstrating how an intermediate layer may be used for routing signals on multiple layers which otherwise would cross on a single layer.

FIG. 9B is an exploded perspective view demonstrating how an upper layer may be used for routing signals for a lower layer.

FIG. 10 is an exploded perspective view of a multi-layer microprocessor having an additional layer of random access memory.

FIG. 11 is an exploded perspective view of a multi-layered bit-sliced microprocessor.

FIG. 12 is an exploded perspective view of a layered multi-processor system.

FIG. 13 is an exploded perspective view of a multi-layer microprocessor, with random access memory on an upper layer and a programmable logic device on the lower layer.

controller 204, activates and deactivates various buffers 116 in accordance with bus arbitration protocol.

A typical microprocessor is programmed through the use of software. Software is a series of logical instructions encoded by a compiler into a format which the controller 204 understands. After the microprocessor is reset, software is downloaded into internal random access memory 108, or off-chip random access memory. Alternatively, the software may be supplied by a pre-programmed read only memory.

Initially, the program counter register 208 contains the address of the instruction to be fetched. The address is moved from the program counter register 208 to the memory address register 210 and the program counter register 208 is incremented. After clocking the contents of the memory address register 210 onto the address bus 224, the controller 204 asserts a memory read signal, which places the data word stored in memory to be available on the data bus 114. The controller 204 activates the appropriate control signals so that the data word is passed through the 'a' side of the arithmetic logic unit 102, through the shift register 106, and into the instruction register 206.

Control decisions are made based upon the contents of the instruction register 206. For example, an instruction could command the controller 204 to add the contents of the accumulator register 104 to the contents of a particular location in random access memory 108, and to store the result in the accumulator register 104. The controller 204 would first address that location in random access memory 108, clocking its contents onto the data bus 114. The controller 204 would then have the arithmetic logic unit 102 add the word on the data bus with the contents of the accumulator register 104. The result would be clocked out of the shift register 106

arithmetic logic unit 102, on the second layer 100, receives status words from the status register 202 over a inter-layer connector 150. The controller 204 supplies various control signals, clock signals and memory read/write signals to the second layer by inter-layer connector 160. The address bus 224 and shift register output bus 112 are distributed to both layers through the use of inter-layer connectors 154 and 158 respectively.

The size of the inter-layer connectors 140 is quite small, relative to the size of the bonding pads 226. Not much larger than the minimum feature size, the connector facilitates inter-layer communication without reserving much real estate on the die. An inter-layer connector is illustrated schematically in FIG. 2. Each shift register output is routed to a metal terminal 252. A hole 256 is routed through the second layer exposing a metal path on the first layer. A metal layer 254, is implanted in the hole, providing electrical contact between the terminal 252 on the second crystalline layer and the exposed metal path on the first layer. Inter-layer connection is achieved with a minimal loss of die space.

FIGS. 3A-3H illustrate an Isolated Silicon Epitaxy (ISE) process, used to form silicon-on-insulator (SOI) films in which the microprocessor circuitry is fabricated. Note that any number of techniques can be employed to provide a thin film of single crystal silicon. An SOI structure, such as that shown in FIG. 3A, includes a substrate 300 and an insulator 302 (for example silicon dioxide) that is grown or deposited on the substrate 300. A thin single layer crystalline of silicon 304 is formed over the insulator 302. The insulator 302 is thus buried beneath the silicon surface layer. For the case of ISE SOI structures, the top

partially or completely fabricated prior to transfer. The crystallization and release procedures including the cleavage of laterally grown epitaxial films for transfer (CLEFT) approach are described more fully in U.S. Pat No. 4,727,047 incorporated herein by reference. The chemical epitaxial liftoff (CEL) approach is described more fully in U.S. Pat. Nos. 4,846,931 and 4,883,561 both incorporated herein by reference. Both the CLEFT and CEL techniques permit the reuse of the substrate, leading to reduced cost compared to other approaches in which the substrates are consumed. By combining thin film release techniques with SOI wafers, high quality films and circuits can be formed on glass.

Note that in FIG. 1, the fabricated components and interconnects on the second layer film 100 face the first layer 200 and the components, interconnects and bonding pads on the first layer 200 are above the substrate 220, facing the second layer 100. This example presents the single transfer process method of multi-layered fabrication.

In the single transfer process, the thin film transistors of adjacent layers face each other. A detailed cross-sectional view of a circuit layered by use of the single transfer process is presented in FIG. 4A. The substrate for the first layer 200 supports an insulating layer 400, upon which is fabricated logic blocks comprising a plurality of transistors 408, 410. The second layer 100 may be separated from its substrate by the method described more fully in U.S. Pat. No. 5,206,749 incorporated herein by reference, or by the CLEFT and CEL approaches cited previously. Supported by its thin silicon dioxide layer 404, the second layer 100 is turned so that its transistors 412 face the transistors 408, 410 of the first layer 200. It is then aligned for proper placement and affixed to the first

Masterbond Inc. It is desirable that the adhesive have the following characteristics:

Good adhesion to glass, oxides, metals, nitrides;
No reactions with glass, metals, oxides, nitrides;
Low shrinkage;
Low warp/stress;
Able to tolerate acids at 100C for extended periods without lifting, losing adhesion, or degrading;
Able to withstand at least 180°C for 2 hours without degradation and withstand 165° for 48 hours without degradation;
change;
Good resistance to acids and solvents;
Able to tolerate dicing and heating steps (including an acid etch step with no lifting);
Low viscosity to allow thin adhesive films; and
Ability to be vacuum degassed to eliminate all bubbles.

In general, the cycloaliphatic anhydrides meet all of the above criteria. The epoxy preferably has a low cure temperature to minimize stress from thermal expansion MIS match, a very low ion content (<5ppm) and low shrinkage.

The wafer, or tile, is attached, using the adhesive, to a glass superstrate. For example EP 112 is an adhesive, that is vacuum degassed to eliminate all bubbles. This sandwich structure is then cured at a low temperature of about 130°C-130°C for 4-8 hours which causes the adhesive to gel and minimizes the thermal mismatch characteristics. Then the adhesive is fully cured at a higher temperature of about 160°C for about 8 hours. This cure assures that the bonds are fully matured. Without this cure, the adhesive will not stand up to any required subsequent acid etching step.

After all the necessary circuits are formed, as above, on transfer bodies, they may now be diced and tiled onto a common module body to perform a combined function, such as a microprocessor.

After all the circuits are registered and adhered to the module body, the superstrate is removed using a suitable etchant.

Interconnection of circuits is achieved during registration with solder bumps that extend through the adhesive or by direct laser writing or by metallization and photolithography, or as described elsewhere herein where necessary.

A preferred embodiment of the single transfer method is presented in FIG. 4B. Again, as in FIG. 4A, in a single transfer process, adjacent layers 200, 100 are aligned so that their transistors 408, 412 face each other. The layers are again affixed with heat conducting, electrically insulating epoxy. The silicon dioxide 434 on the second layer is cut, exposing the second layer 100 transistor 412 metal pad 420 and the epoxy area covering the first layer 200 metal pad 418. A hole 430 is etched through the cured epoxy layer 402 exposing the metal pad 418. A metallization layer 432 is used to electrically connect the exposed metal pads 418, 420. This method reduces the patterning complexity, and shortens the length of the metal line in comparison to the method described by FIG 4A. In some applications, the FIG. 4A. method could be used to insulate the metal layer from components.

Another method of layering involves a two-step process referred to as double transfer. As shown in FIG. 4C, in a double transfer process the layers are aligned so that their transistors are stacked, rather than facing each other as in the single transfer method.

transfer structures and can be used in structures having three or more layers in a cascade structure.

FIG. 5A presents a cross-sectional view of multi-layer shielding. An insulating layer 502 is applied over transistor 408 before the epoxy 402 is applied. A conducting metal layer 504 is patterned over the insulating layer 502 to provide for a shielding path. This path shields transistor 408 on the first layer 200 from transistor 412 on the second layer 100, reducing the threat of problems associated with thermal degradation, cross-talk, and electro-magnetic interference.

Another method of shielding is shown in FIG. 5B. The first layer 200 is shielded from the third layer 500 by an electrically conductive second layer 100. A metal layer 506 is patterned on the second layer 100, shielding transistor 408 on the first layer 200 from transistor 412 on the third layer 500. The conductive second layer 100 is aligned and epoxied over the first layer 200 and after the epoxy cures, the third layer 500 is aligned and epoxied over the second layer 100. A double transfer process is shown, but a single transfer process may be used as well. Depending on the application, power or ground would be applied to the electrically shielding layer.

FIG. 6 shows a first 200 and second 100 wafer being aligned in a single transfer process. The first wafer 200 comprises an array of individual circuit elements 520, which are to be electrically connected to the array of circuit elements 510 on the second wafer 100.

FIG. 7 is a progressional flow diagram of the layering process. The wafer film is first removed from the wafer substrate. Layer by layer, each film is aligned, epoxied, and electrically connected to the film

and up to the third layer again by the use of an inter-layer connector over the lines connecting A and A' to logic block B' 628. The use of an intermediate routing layer provides interconnect between logic blocks on separate layers while reducing the space consumed by complicated routing patterns.

FIG 9B shows how an additional routing layer may be used in connecting two logic blocks fabricated on the same layer. Logic block A 640 is to communicate with logic block B 642 on the same layer, but blocks A 640 and B 642 are separated by logic block C 644. In the single layer context, the signals would have to be routed around logic block C 644. In a multi-layer context, the signal could be routed from A 640 up to the second layer by the use of an inter-layer connector 646 continuing directly over logic block C 650 over to inter-layer connector 648, back down to logic block B 642.

An individual logic block may be fabricated on several layers, with inter-layer connectors providing for interconnect between the subcomponents of the logic block. For example, an eight bit shift register, instead of being fabricated on a single layer, could be fabricated so that it is partitioned onto eight layers, with one bit on each layer, or it could be partitioned onto four layers, with two bits on each layer. This affords greater flexibility in placing the logic blocks and frees up space for inter-connect routing.

As shown in FIG. 10, an additional layer or several layers of random access memory may be stacked on top of the multi-layer microprocessor. The address bus 252, data bus 254, and control bus 250 are routed up to the random access memory by the use of inter-layer connectors. This configuration results in reduced

second 804 and third 806 layers comprise a multi-layer microprocessor, with random access memory on the fourth layer 808. The programmable logic layer 802 can be programmed to provide for user-defined communication protocol between the microprocessor and any off-chip resources. The array 802 can be formed in any of the layers of a multilayer structure as described elsewhere herein.

As shown in FIG. 14, a light-emitting diode array may be mounted as the top layer in a multi-layer configuration. The x-axis driver circuitry 826 is fabricated on the second layer and is connected to the LED array by the use of inter-layer connector 834. The y-axis driver circuitry 828 in the same way is connected to the LED array layer 840 by inter-layer connector 832. The driver circuits receive information to be displayed from the data bus 824. In preferred embodiments these LED elements or arrays can be used to form integrated displays or alternatively can be used along with fiber optics to optically interconnect different layers of the structure. The fabrication of bulk or thin film III-V semiconductor materials which are transferred to form LED elements, arrays and circuit elements is described in greater detail in U.S. Serial No. 07/643,552 filed on january 18, 1991 which is incorporated herein by reference. The formation of composite structures including GaAs on silicon structures is also described in the above-referenced incorporated application.

Film segments may be arranged side by side on top of a single layer. In FIG. 15, segments 902 and 904 are layered over segment 900. The segments can communicate directly by the use of a metallization path 910 etched directly over the epoxy layer, or they may communicate by the use of inter-layer connectors 908. Another segment 906 may bridge the segments 902 and 904 with

essentially single-crystal recrystallized silicon, from which CMOS circuits are be fabricated.

Note that for the purposes of the present application, the term "essentially" single crystal means a film in which a majority of crystals show a common crystalline orientation and extend over a cross-sectional area in a plane of the film for at least 0.1 cm^2, and preferably, in the range of 0.5 - 1.0 cm^2, or more. The term also includes completely single crystal Si.

After the devices have been processed and the circuit layers tested and repaired, as required, the next step in the process is to transfer the silicon pixel circuit film to a common module, either directly, or by a double transfer from substrate to carrier and then to the common module. A double transfer approach is illustrated and described in greater detail in U.S. Serial No. 07/874,588 filed on April 24, 1992 which is incorporated herein by reference.

In order to make connections between the layers of circuits, openings or via holes are defined by appropriate etchants in order to expose contact areas on the two circuit layers. All of the oxide is etched in buffered HF using photoresist as a mask while the adhesive can be etched in oxygen plasma or by reactive ion etching (RIE) using the previously etched oxide as a mask. When using RIE, the side walls can be made vertical and the holes completely filled. Once these via holes have been opened in the bonding layer, they can be filled with metal in order to make the contact from layer to layer. The layer to layer interconnections are explained in detail elsewhere in the present application. The adhesive layer between the superposed circuits must be kept very thin, a few

Tracon, Masterbond, and Epotek all make a number of versions of heat conductive epoxies. The highest conductivities are achieved by filling an epoxy resin with various materials including alumina and aluminum nitride. Hitachi also makes a diamond filled epoxy. All the alumina and aluminum nitride filled epoxies are opaque due to the conductive particles used as fillers. They can be cured at room temperature or at elevated temperatures. The aluminum nitride filled epoxies have thermal conductivities of ~3.6 (W^{-1}) (m^{-1}) $(°K^{-1})$. Aluminum oxide filled epoxies are in the 1.44 -21.6 range. Diamond filled epoxies are the best of all. These filled epoxies can be made to accommodate temperatures up to 250°C. The aluminum nitride particle size is 5 μm or greater. Aluminum oxide particle size can be made much smaller so thinner bondlines are possible. Some trade names are Masterbond EP21, Supreme 10, Tracon 2151, Castall E340 series, Epotek H62, H70E. Also, silicon carbide filled epoxies can be used.

It is noted that the filled epoxies sampled are generally viscous, opaque pastes such that it may be difficult to obtain very thin (<5 μm) bondlines. Medium thermal conductance in the 0.85-1.44 (W) (m^{-1}) $(°K^{-1})$ range can be achieved without fillers. These epoxies are of slightly lower viscosity, can be put on thinner and are preferable if the conductance is high enough. Another option is to coat the devices with a thin diamond like film or a conductive ceramic like aluminum nitride to facilitate heat removal. This decreases the thermal conductance criteria for the epoxy, allowing the use of a lower viscosity epoxy in order to achieve the thin bondlines necessary for layer to layer interconnections.

layer 916 which is bonded to the first layer using the single transfer process described in conjunction with FIG. 9A. In a single transfer process, the transistors 922 are supported by a silicon dioxide layer 930 and bonded to the first layer 918 using epoxy 928 as described above.

As shown in FIG. 16B, a small opening 932 is formed in silicon dioxide layer 930 directly above metal pad 920A of the transistor 920. Using the silicon dioxide layer 930 as a mask, an anisotropic etchant is used to expose the metal pad 920A of transistor 920, a shown in FIG. 16C. The silicon dioxide 930 is cut for a second time as shown in FIG. 16D, forming a hole 934 over the metal pad 922A of the second layer transistor 922 and exposing a wider area 936 over the hole 932. In FIG. 16E, the hole 936 over metal pad 920A of the transistor 920 is filled with an epoxy 938 which is electrically and thermally conductive. The epoxy can have silver dispersed therein to provide the desired level of electrical and thermal conductivity. In FIG. 16F, a metallization layer 940 is formed over the conductive epoxy 938 and hole 934. This metallization layer 940 provides electrical contact between metal pad 920A of the first layer transistor 920 and metal pad 922A of the second layer transistor 922.

This method can be used to interconnect adjacent or multiple stacked device or routing layers, or can be used to connect devices to bonding pads on adjacent layers. This method provides a simple inexpensive process for interconnecting device layers with high yield with improved mechanical and thermal characteristics.

Claims

We claim:

1. A data processing device comprising;

a first circuit layer formed in a semiconductor material and having a controller in the first circuit layer to control a data processing operation;

a second circuit layer formed in a semiconductor material and having a logic unit in the second circuit layer that is connected with and controlled by the controller; and

an adhesive layer positioned between and securing the first circuit layer with the second circuit layer, the adhesive layer having interconnects extending between the first circuit layer and the second circuit layer to conduct control signals between the controller and the logic unit.

2. The data processing device of Claim 1 wherein the first circuit layer further comprises a memory.

3. The data processing device of Claim 1 wherein the second circuit layer further comprises a memory.

4. The data processing device of Claim 1 further comprising a third circuit layer connected by interconnects with the second circuit layer, the interconnects extending through a second adhesive layer that secures the third circuit layer to the second circuit layer.

11. The method of Claim 10 further comprising forming a controller in the first circuit or the second circuit.

12. The method of Claim 10 further comprising forming a memory in the first circuit or the second circuit.

13. The method of Claim 10 further comprising bonding the first circuit layer to the second circuit layer with a polymeric adhesive.

14. The method of Claim 10 further comprising forming the second circuit in a thin film semiconductor layer on an insulating substrate.

15. The method of Claim 14 further comprising transferring the thin film semiconductor layer and attached insulating layer onto the first layer of semiconductor layer.

16. The method of Claim 10 wherein the first layer of semiconductor material comprises a bulk semiconductor wafer.

17. The method of Claim 10 wherein the first circuit layer or the second circuit layer comprises silicon.

18. The method of Claim 10 wherein the first circuit layer or the second circuit layer comprises a III-V material.

19. The method of Claim 10 further comprising forming a third circuit layer over the second circuit layer.

25. The data processing device of Claim 21 wherein the adhesive layer comprises a polymeric material.

26. The data processing device of Claim 21 wherein the adhesive layer comprises a thermally conductive epoxy.

27. The data processing device of Claim 21 wherein the adhesive layer further comprises a particulate filler.

28. The data processing device of Claim 27 wherein the particulate filler comprises metallic particles.

29. The data processing device of Claim 21 wherein the first circuit layer comprises an arithmetic logic unit.

30. A method of fabricating a data processor comprising:

forming a first circuit of a data processor in a first layer of semiconductor material;

forming a light emitting device in a second layer of semiconductor material;

bonding the second layer to the first layer with a bonding layer; and

connecting the first data processor circuit with the light emitting device light emitting device with interconnects extending through the bonding layer such that data processor control signals can be conducted from the first data processor circuit to the light emitting device.

31. The method of Claim 30 further comprising forming a controller in the first circuit.

a first circuit layer formed in a semiconductor material and having a controller and logic unit in the first circuit layer to control and perform a data processing operation;

a second circuit layer formed in a semiconductor material and having a second controller and a second logic unit in the second circuit to control and perform a second data processing operation; and

an adhesive layer positioned between and securing the first circuit layer with the second circuit layer, the adhesive layer having interconnects extending between the first circuit layer and the second circuit layer to conduct control signals between the first circuit layer and the second circuit layer.

42. The processing device of Claim 41 wherein the first circuit layer further comprises a memory.

43. The data processing device of Claim 41 wherein the second circuit layer further comprises a memory.

44. The data processing device of Claim 41 further comprising a third circuit layer connected by interconnects with the second circuit layer, the interconnects extending through a second adhesive layer that secures the third circuit layer to the second circuit layer.

45. The processing device of Claim 41 wherein the adhesive layer comprises a polymeric material.

layer to conduct signals between the first circuit layer and the second circuit layer.

51. The data processing device of Claim 50 wherein the first circuit layer further comprises a memory.

52. The data processing device of Claim 50 wherein the second circuit layer further comprises a memory.

53. The data processing device of Claim 50 further comprising a third circuit layer connected by interconnects with the second circuit layer, the interconnects extending through a second adhesive layer that secures the third circuit layer to the second circuit layer.

54. The data processing device of Claim 50 wherein the adhesive layer comprises a polymeric material.

55. The data processing device of Claim 50 wherein the adhesive layer comprises a thermally conductive epoxy.

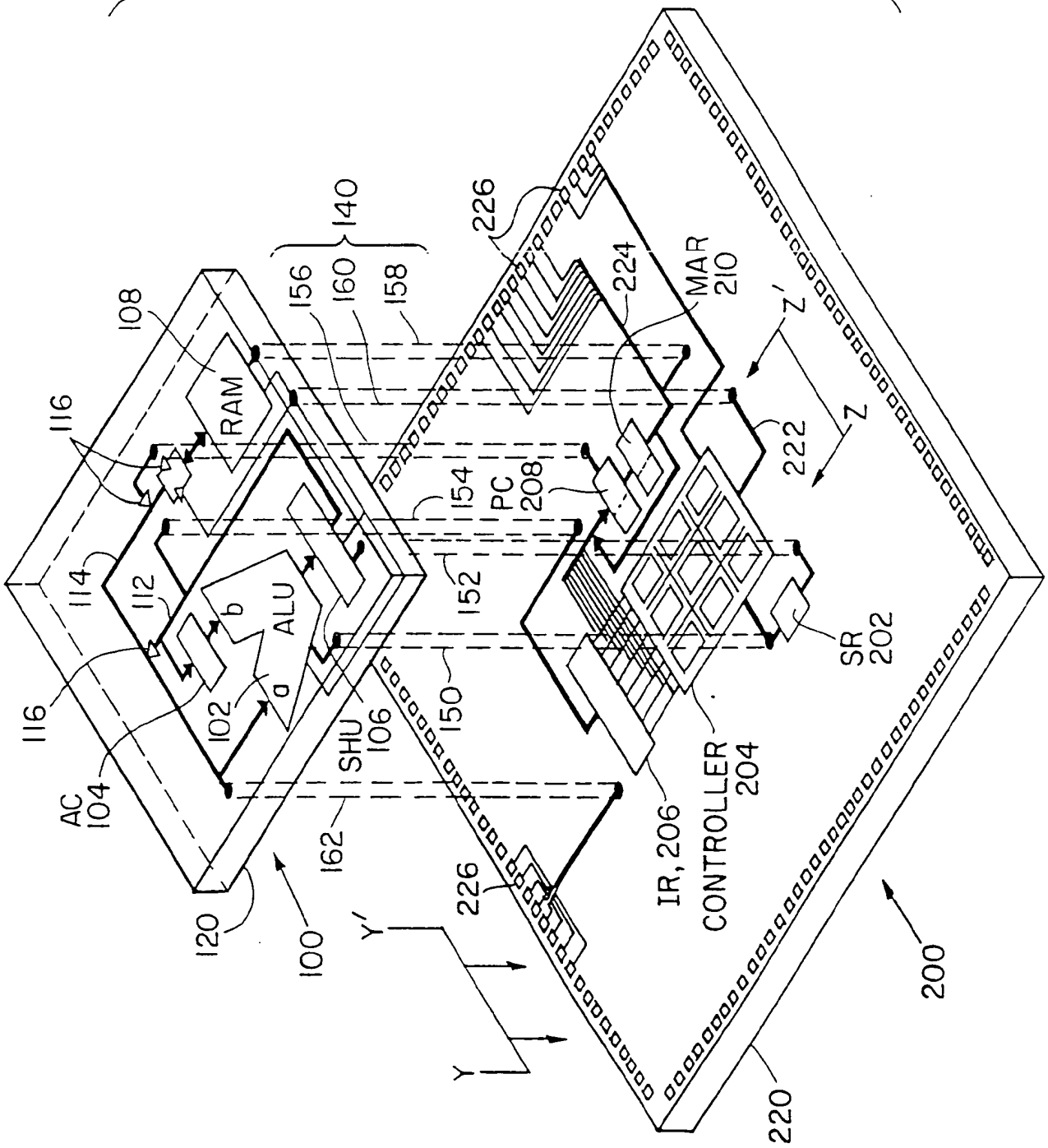
56. The data processing device of Claim 50 wherein the logic unit circuit comprises an arithmetic logic unit.

57. A method of fabricating a data processor comprising:

forming a first circuit of a data processor in a first layer of semiconductor material;

forming a circuit routing layer and bonding the circuit routing layer to the first circuit layer;

FIG. 1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158
226
224
MAR
210
108
RAM
116
154
PC
208
222
Z'
Z
114
112
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152
SR
202
116
102
a
SHU
106
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104
162
226
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CONTROLLER
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120
100
Y'
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220
200

FIG. 3A

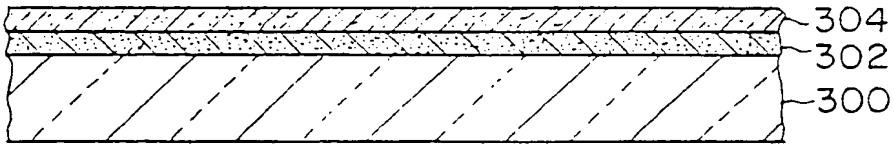


FIG. 3B

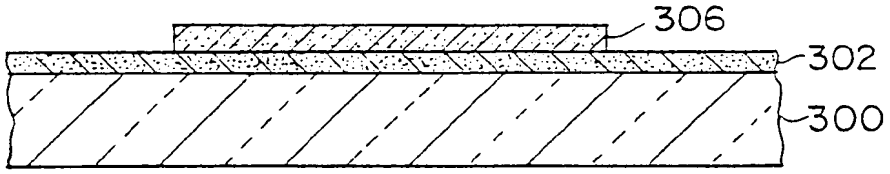


FIG. 3C

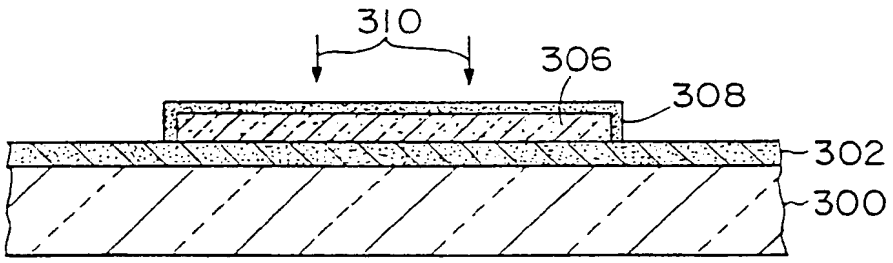


FIG. 3D

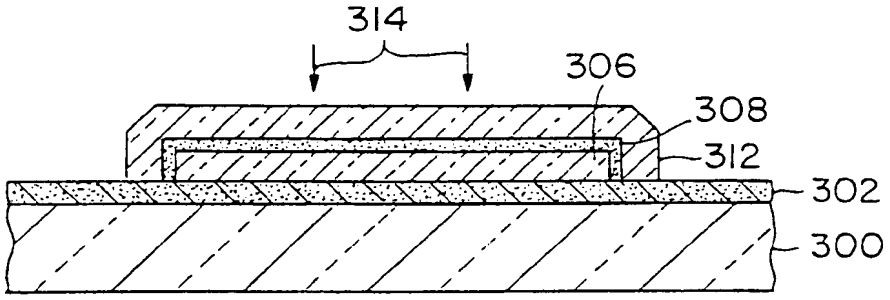
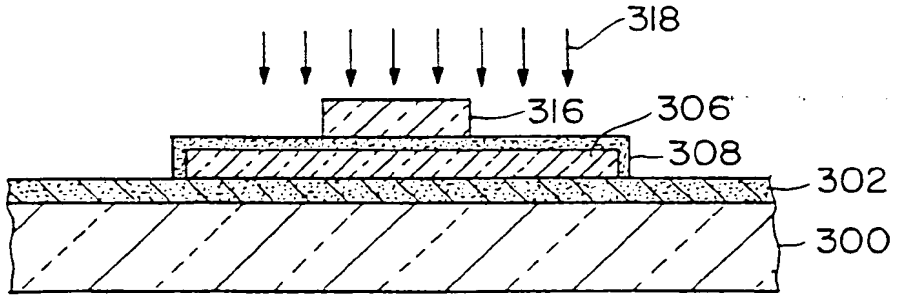


FIG. 3E



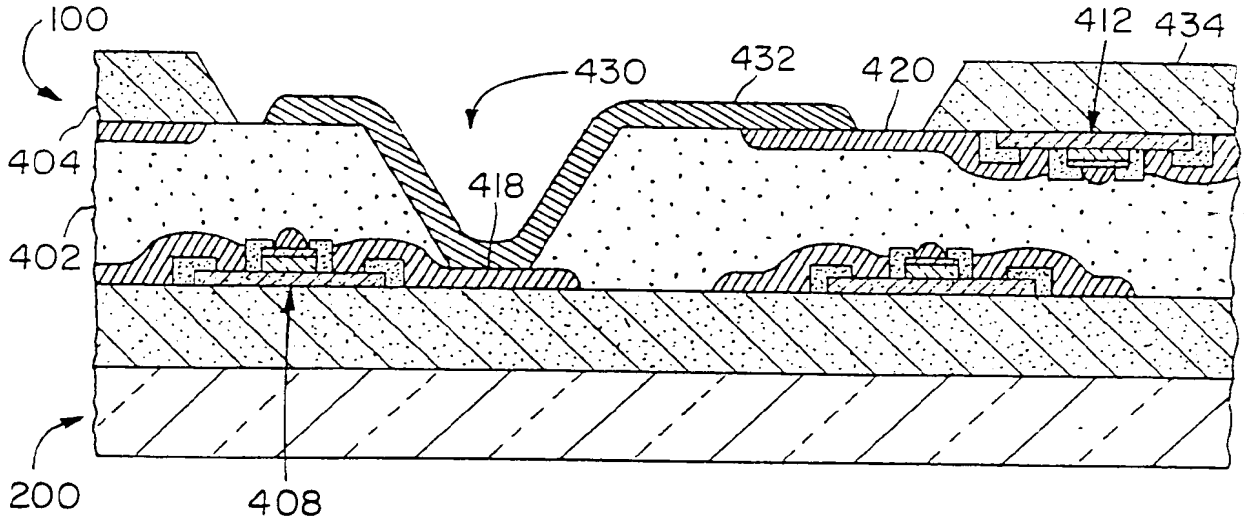


FIG. 4B

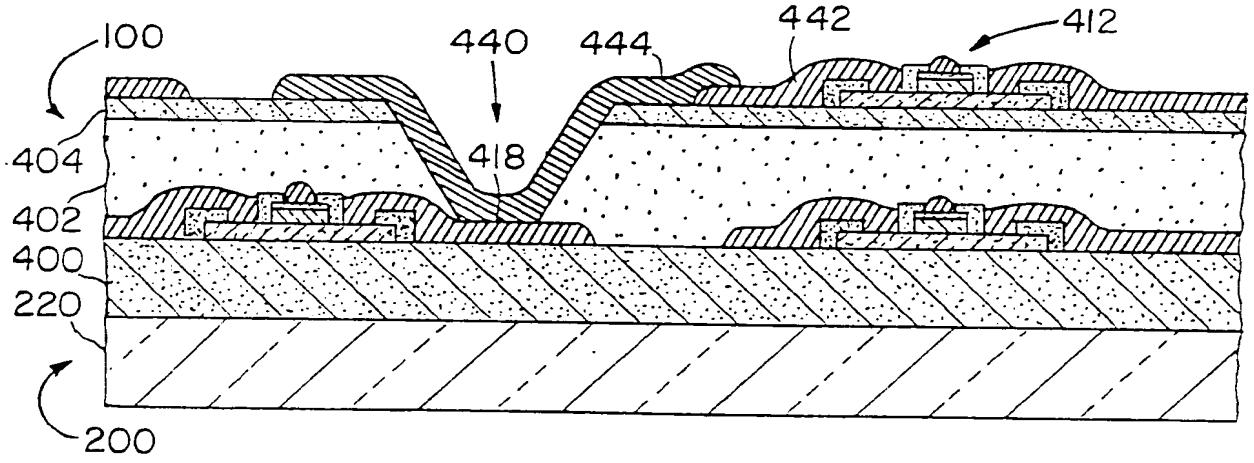


FIG. 4C

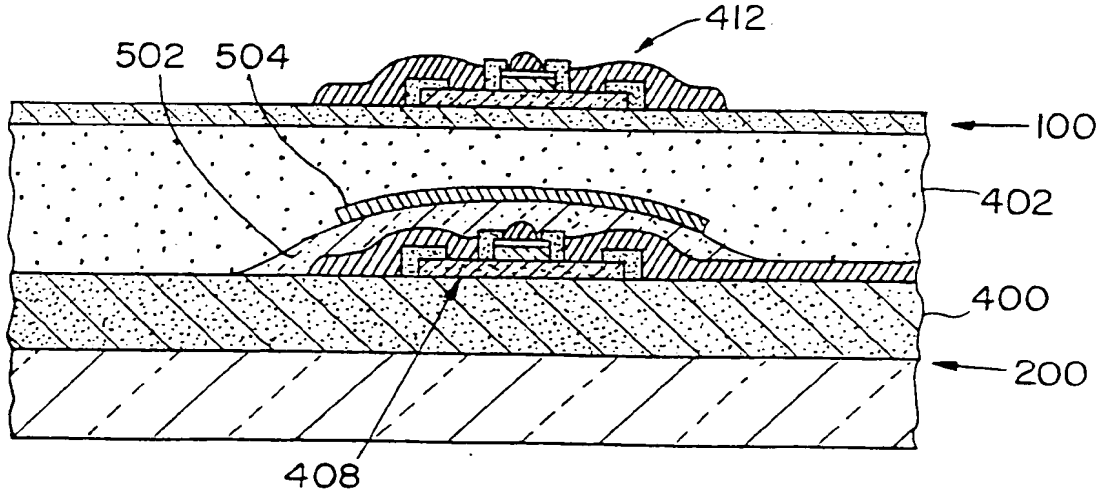


FIG. 5A

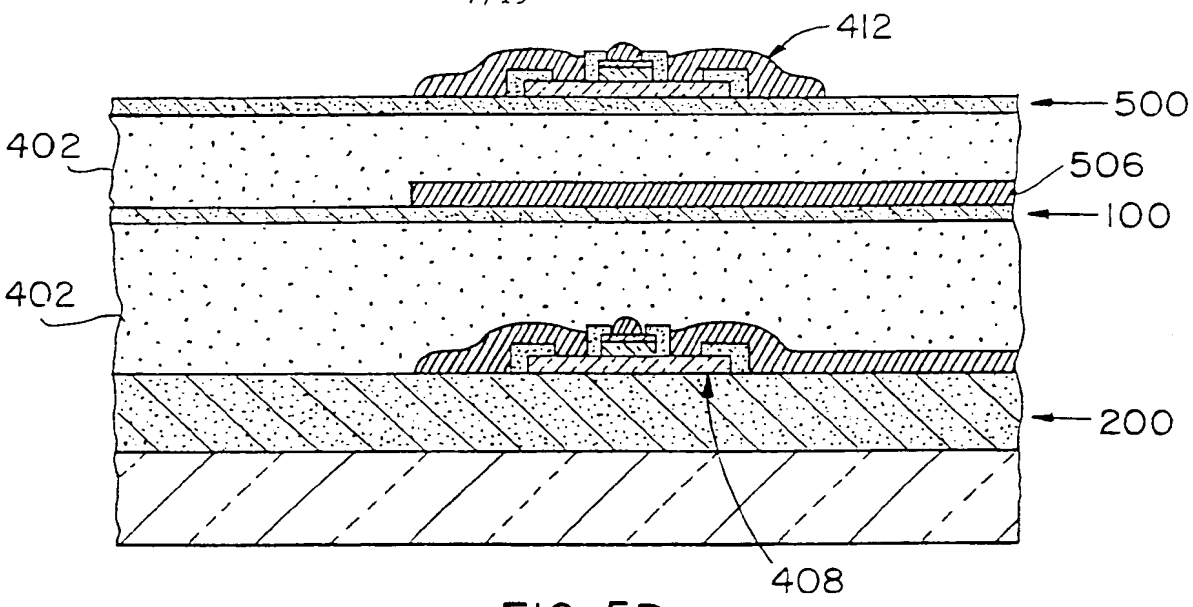


FIG. 5B

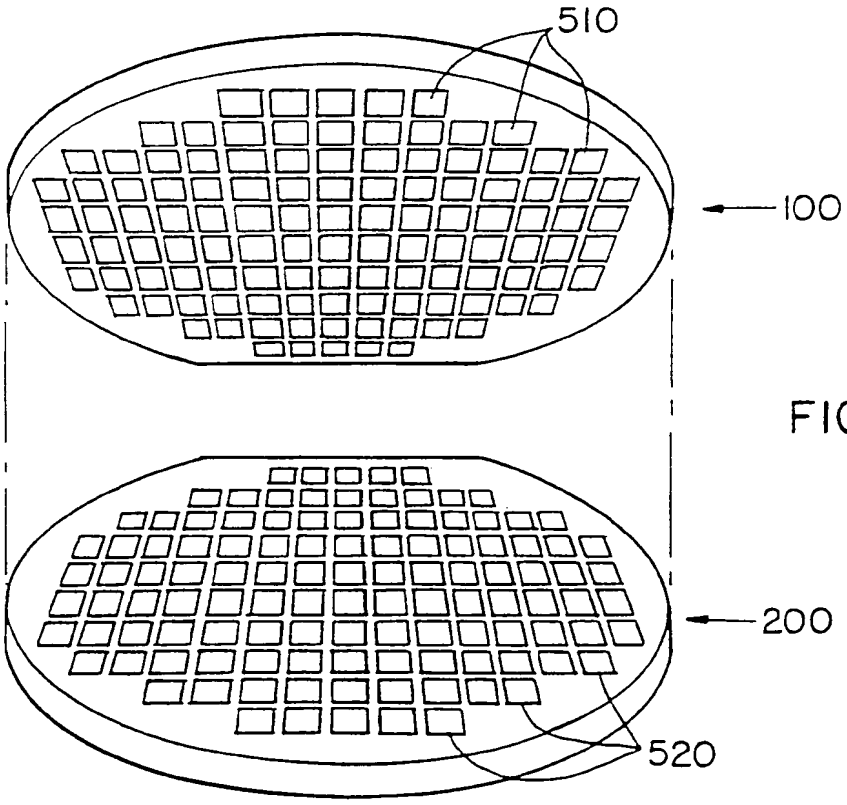


FIG. 6

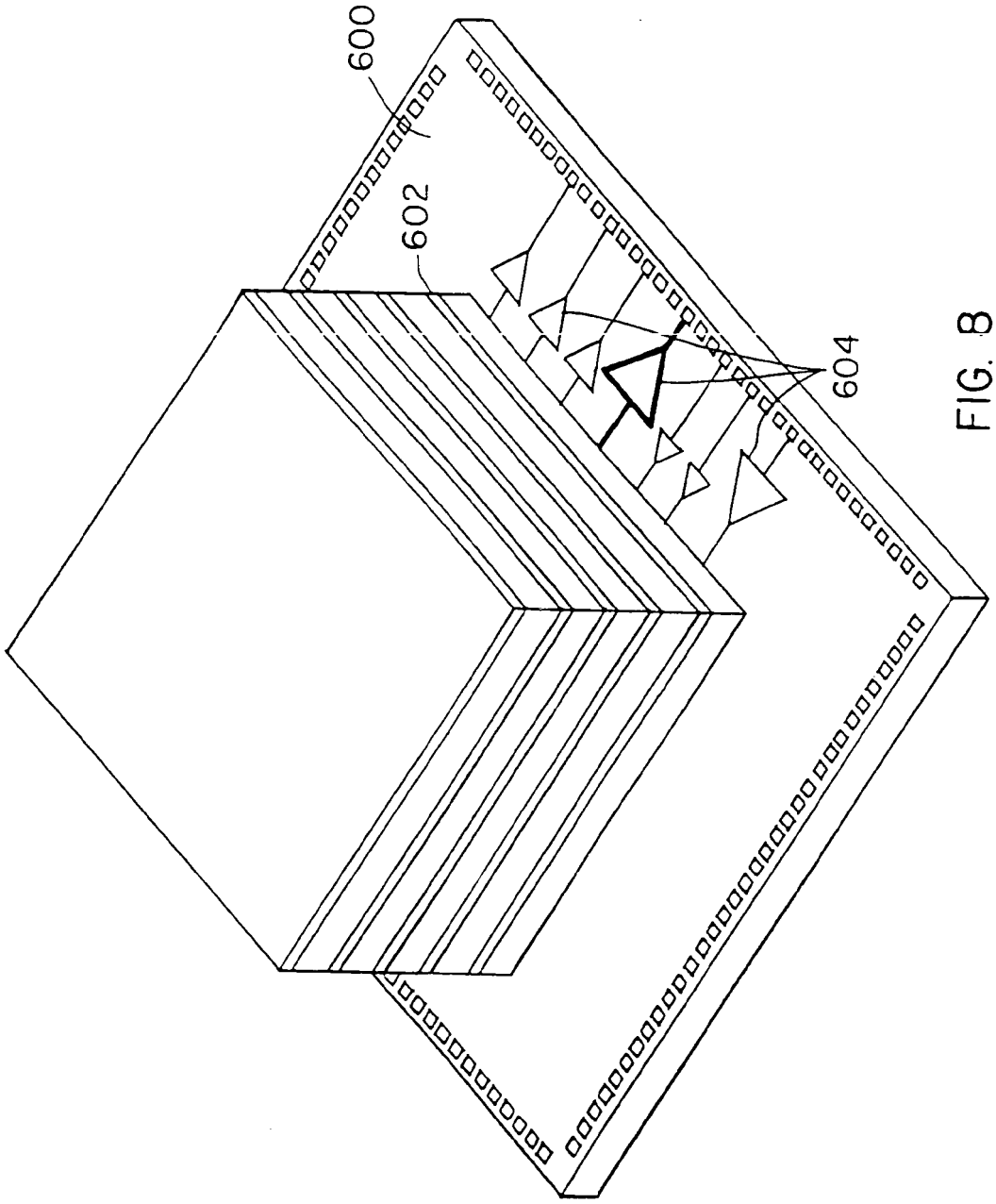


FIG. 8

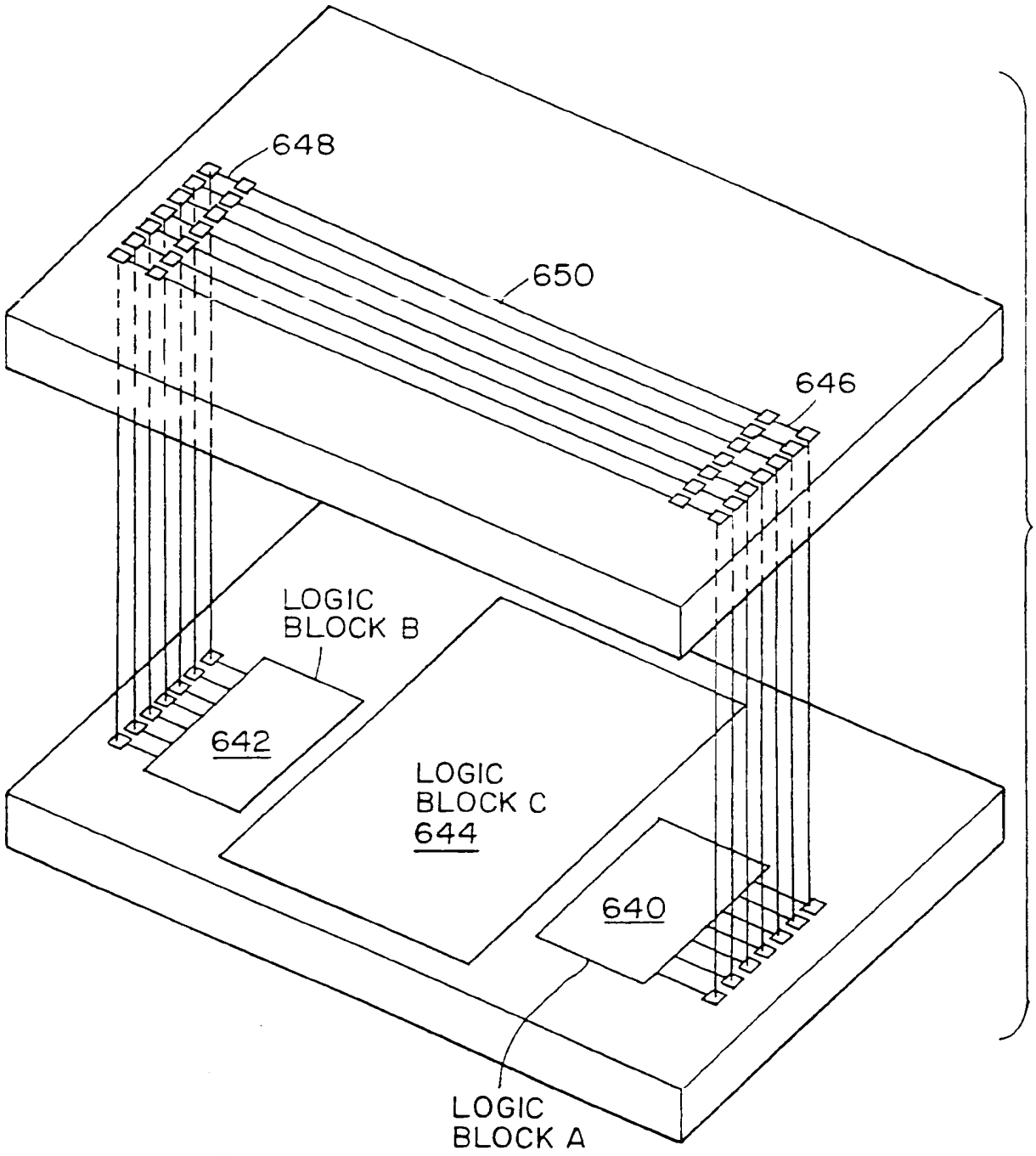

648
650
646
LOGIC
BLOCK B
642
LOGIC
BLOCK C
644
640
LOGIC
BLOCK A

FIG. 9B

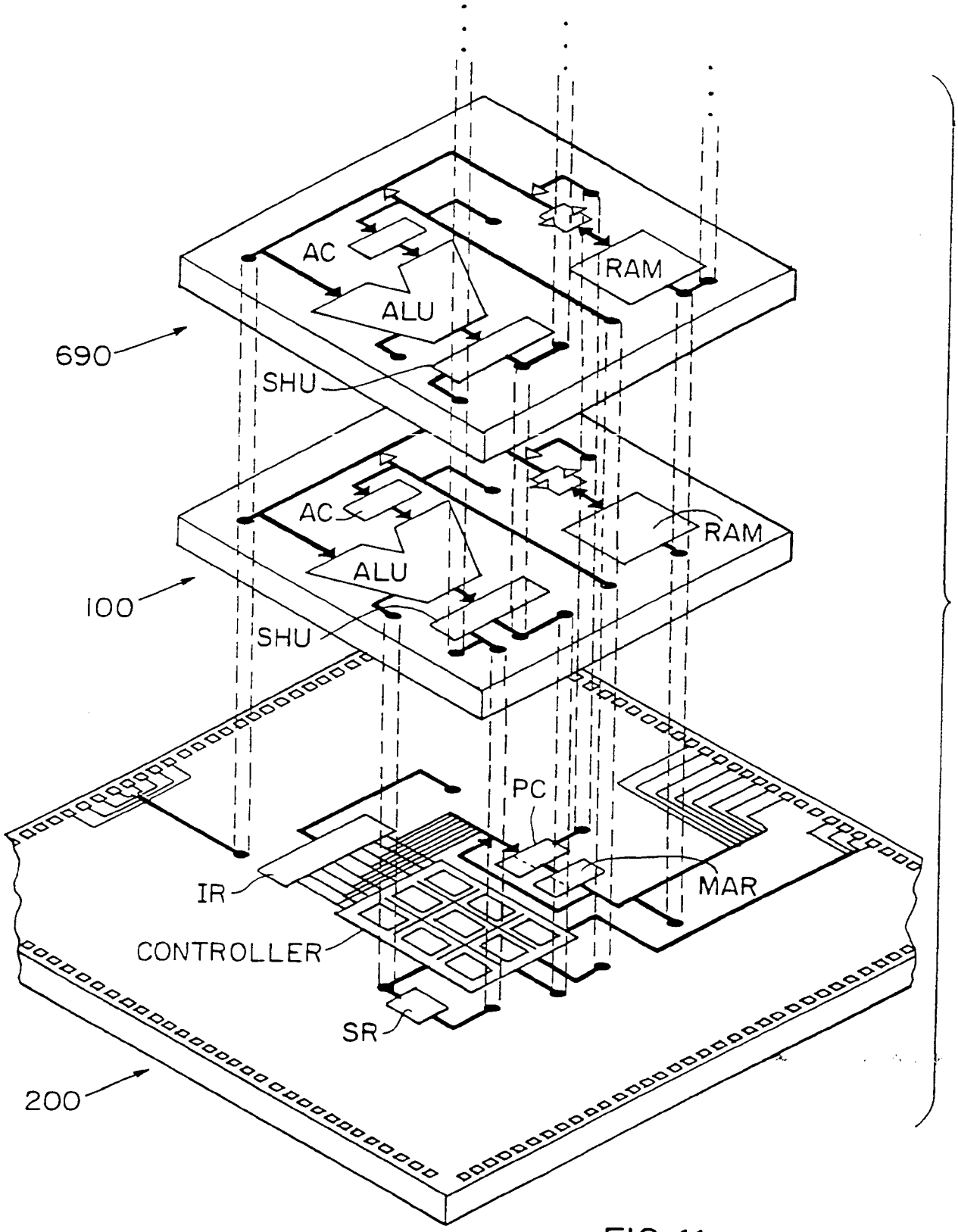

AC
ALU
RAM
690
SHU
AC
ALU
RAM
100
SHU
PC
IR
MAR
CONTROLLER
SR
200

FIG. 11

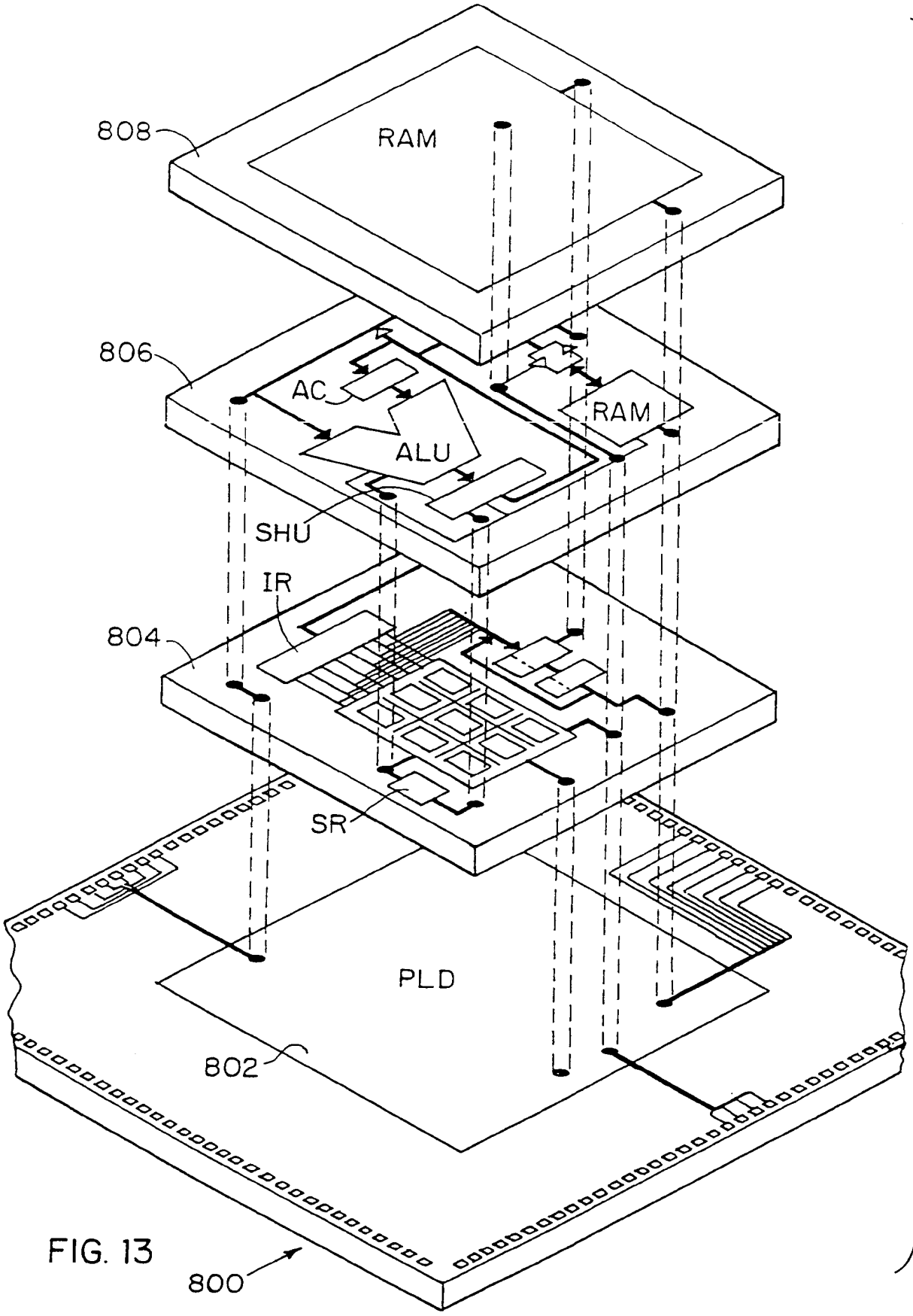
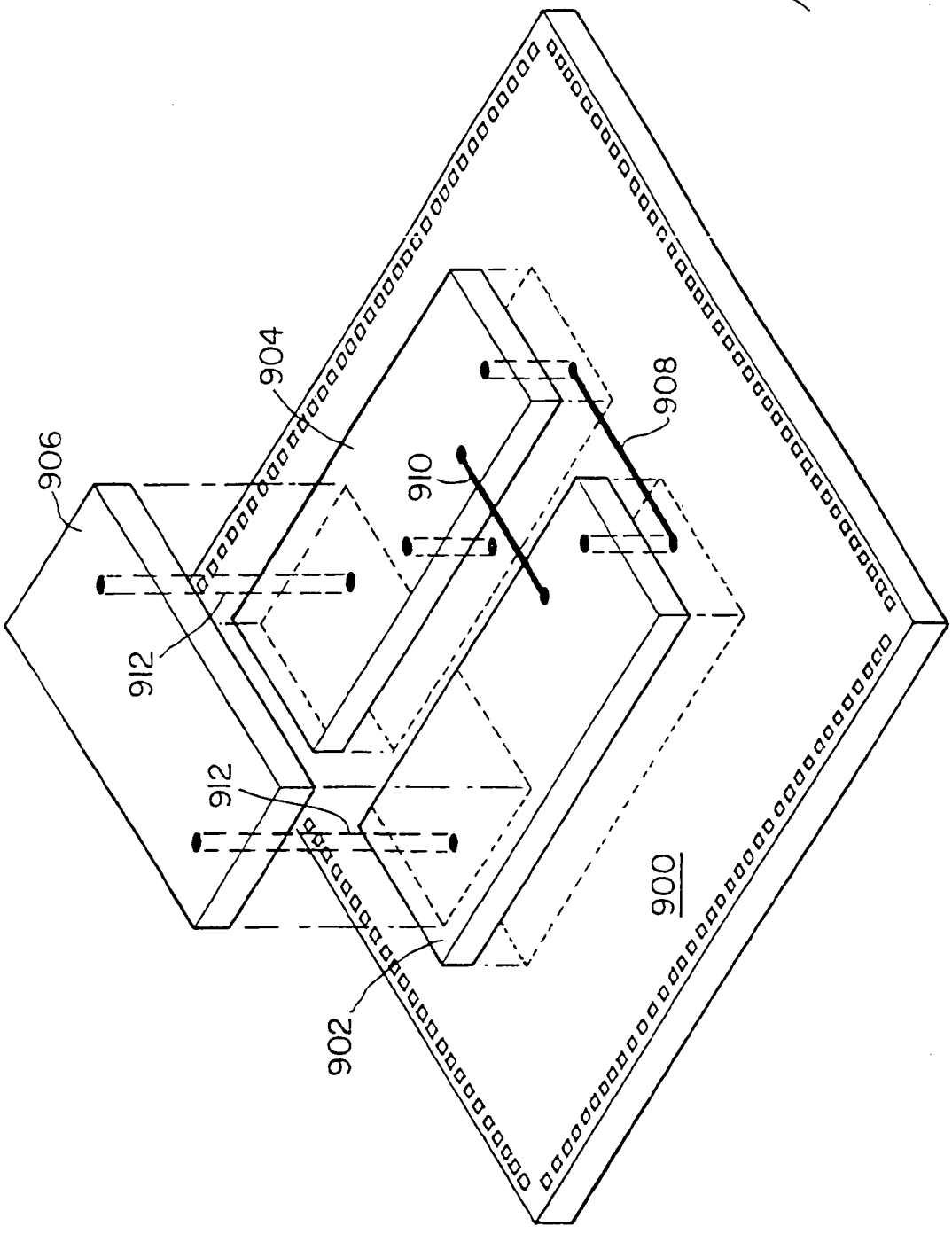


FIG. 13

FIG. 15



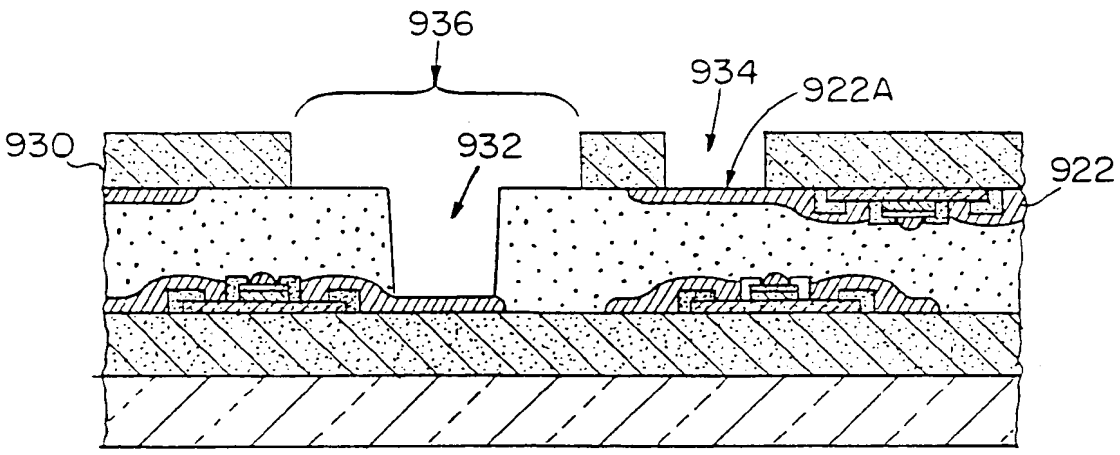


FIG. 16D

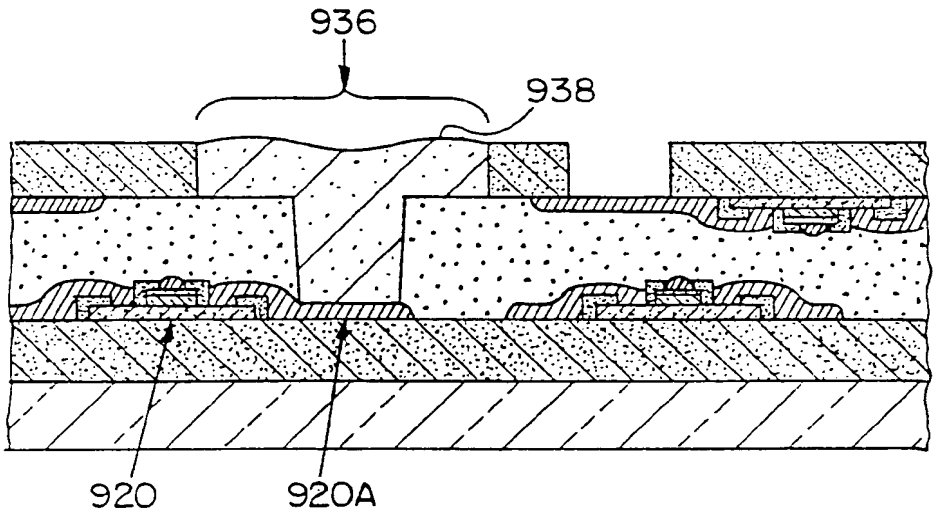


FIG. 16E

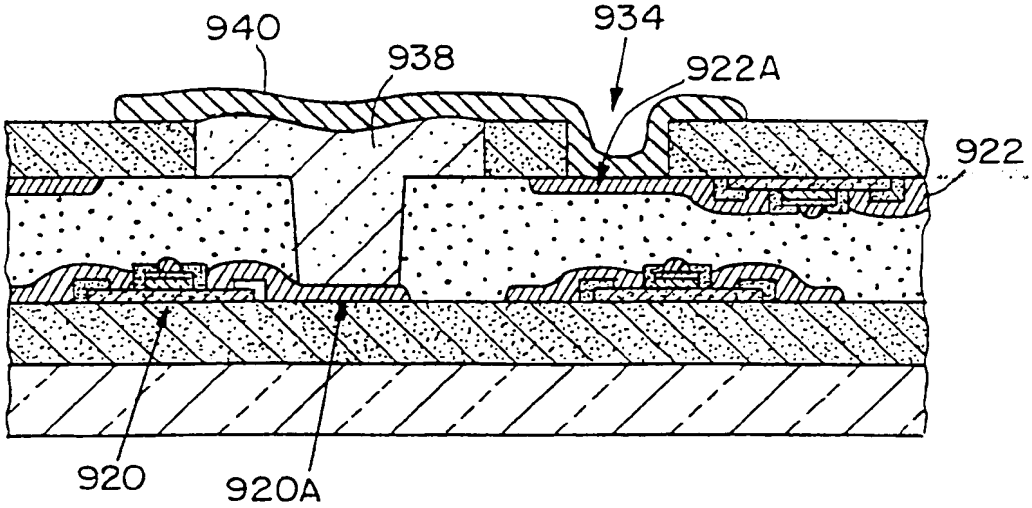


FIG. 16F

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,4 897 708 (CLEMENTS) 30 January 1990 see column 3, line 6 - column 4, line 43	1

Form PCT/ISA/210 (continuation of second sheet) (July 1992)